# Projekt ( Differential Pairs )

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Indholdsfortegnelse

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## Hvad skal jeg?

Designe en differential amplifier, som jeg kan bruge i flere forskellige konfiguration såsom operational transconductance amplifiers and operational amplifiers

## Hvordan kan jeg gribe den her opgave an?

Undersøge operational amplifiers og operational transconductance amplifiers.   
Spørge chatten om den har nogle trin som kunne være gode at følge, og hvad jeg skal prøve at opnå.

1. Hvilket setup vil jeg lave?
2. Start i det små, byg da på ( Det rimer :O )
   1. Lav differential pair.
   2. Sørg for biasing
   3. Tilføj load / cascode koblinger
   4. Feedback?

Alt imens jeg vil dokumentere mine fremskridt med forklaringer og eller simulationer.   
Test består af:

1. Passer mit gain?
2. Input / output range?
3. Gain / bandwidth?

Hvis nødvendigt, så vil jeg tilpasse specs som størrelser mm.

## Hvad er differential pair

De har en

1. Common mode spænding
2. Differential mode spænding
3. Common mode rejection ratio ( CMRR )

## Objective:

This project is meant for me to try to design and simulate differential pair used in different types of differential amplifiers.

## Introduction?

## Theory

I’m supposed to design for Figure 4.5. That’s where all my calculations will go towards, trying to satisfy criterias, which I will be solving in the following order.



*For my calculations I will start by simplifying everything, and if the results differs too much, I can come back and add complexity to my calculations, to get more precise answers.   
To start with*

When estimating values, I will give a headroom of about 20%.

### Power Supply

The power supply isn’t just about setting the supply, my tasks is here to ensure, that the transistors will all be in saturation. This means finding the dimensions of the transistors that satisfies this.   
Finding the dimension of M1 is easy, as I can just solve that with the bias transistor and it’s lengths.   
M1 is a current mirror with M2, so I can’t just set M1 straightaway, without knowing how much current is needed for the output network to be in saturation.

Et billede, der indeholder Font/skrifttype, tekst, hvid, typografi

Automatisk genereret beskrivelseI can use the fact that the pmos network makes for current mirrors aswell making a relationship between the two currents that adds up to be the tail current

For the threshold and K values, the pmos values are all the same, and the nmos values are all the same, therefore for this current mirror.



Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelseEt billede, der indeholder diagram, Plan, Teknisk tegning, linje/række

Automatisk genereret beskrivelse  
   
   
   
   
So I’ve got an equation for the tail current.   
For simplicity’s sake I choose to ignore all other capacitance than the load capacitor.   
Then I get



Let me go from ground and up, making sure, that all transistors are in saturation.

Then for the saturation region:

Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelse



For the diode connection, the transistor will always be in saturation, as long as it’s   
activated.   
   
With headroom.

Then   
   
  
And   
   
As must be fullfilled for saturation, the larger I can make VDS1, the larger the range in output I can get.

For this to be ensured, VD must then just barely fullfill the need to operate in saturation.

The power supply is easy to implement.   
The voltage source will be set to and I will be grounding VSS

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Automatisk genereret beskrivelse

## Tests

## Conclusion

## References

Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelse

Figur 4.5 a. The differential circuit, that I'm trying to design for

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Automatisk genereret beskrivelseLad mig se på kravene:   
Krav 1:  
Der skal gælde at:  
   
   
Det eneste andet krav jeg stiller til min strømkilde er, at gate spændingen skal opfylde  
   
   
Samt at



Krav 2:   
Jeg ønsker en høj output range. For at det skal ske, så sikrer jeg bare saturation for pmosene plus 20%  
For at sikre en diode koblet transistor saturation, så skal den bare være tilstrækkeligt til at være tændt, deraf navnet diode koblet transistor.

Så har jeg lagt kravet for mit pmos netværk.

Et billede, der indeholder tekst, kvittering, algebra

Automatisk genereret beskrivelse

Krav 3:   
   
   
   
So this is my maximum value Vin.   
   
Substituere formel 3 ind

Substituere formel 2 & 4 ind i uligheden.  
   
   
   
Øvre grænse for Vin.

Den skal også opfylde at   
   
   
   
Substituere formel 2 ind



Så jeg har at   
   
   
Så der ses, at:

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Automatisk genereret beskrivelseSo let me find the widths of the biasing transistors to maximize the range.   
   
   
Substituere formel 3 ind:   
   
   
   
  
Setting both pmos ratios to be equal   
   
   
   
Substituting formular 3 into the equation:

And the relationship between those two currents and   
   
   
  
   
Substituting using formular 7, 8 & 9.

From ratio symmetry Vo should be Vx   
Substituting eq. 4 into the equation and substituting the impedance of the capacitor..

Now I’ve got an equation full of constants and one variable.  
Let me use some standard values.

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Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, skærmbillede, nummer/tal

Automatisk genereret beskrivelse------------------------------------------- Setting standard values --------------------------------------------  
   
   
   
 have I simplified to be 0.

Now substituting the tail current.   
   
   
   
   
   
For low frequencies, the capacitor current is negligible.   
For higher frequencies, the capacitor current starts affecting the circuit.   
For higher ratios, the effects of higher frequencies becomes smaller.

Now this current goes through M4.   
   
And from the inequality of equation 6, I remember that higher VGS causes lower Vin range.   
VGS4 must be at a minimum then   
   
   
   
   
   
Substituting values:   
   
   
   
   
   
   
   
   
   
Which suggest that I should just suggest values for my current sources and adapt my pmos transistors to their sizes.   
Before I start experimenting with the sizes, I miss the relationship to Rbias.

----------------------------------------------- Size experiments ------------------------------------------------   
Setting the size ratio to 10

Supporting   
   
   
   
   
   
   
, so the complex part of the impedance is negligible.

I’ve given VGS4 plenty of headroom, so I think that it will do with rounding up.

Let me do a simulation over a Vin range.

Seems that my configuration can handle the frequencies. The simulation just looks like Dc over a transient analysis of 50us.[[1]](#footnote-1)

I noticed a flaw in my part, as well as a flaw in LTspice part.   
When placing down a pmos4 it’s rotation makes it go from drain at the top, to source at the bottom. It’s reverse of how we usually use mosfets.   
The flaw on my behalf is, that I setup my inputs in the wrong way, making that no current would run through the output side.   
Changing those two steps and getting the result of figure 2, current running through both, and observing vout changing depended on the input. [[2]](#footnote-2)   
After trouble shooting I have a plot. But not a rightful one as I get the small signal gain to be:

So something is wrong. [[3]](#footnote-3)  
  
Looking into it, I’ve found one of the problems atleast.  
The input transistors are running in linear, as

Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelse



For the range of the input to be at its largest, then   
The pmos current mirror and the nmos current source should have VDS be at their minimum.

Maximizing VD1 maximizes Vin.

Giving it some headroom.

For the minimum value of Vin, let me look at, the VDS of m4.

Giving headroom.

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Automatisk genereret beskrivelse  
   
   
   
   
  
   
And I’m supposed to design this for the range to be atleast 0,5V.

And simplification of tail current to reference.   
   
   
As I now my tail current.   
   
   
And then I’ve made equations for all transistors in the circuit.

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Automatisk genereret beskrivelseFinding expression for VSD5 and VG4, such that I can find the numerical values for the boundary.   
, so I want the lowest VSG5.



Configuring the network such that, by setting the sizes of the pmoses to be equal.

Substituting that into equation 7.   
   
   
Substituting that into equation 10.   
   
   
   
Substituting back into boundary

Et billede, der indeholder tekst, Font/skrifttype, skærmbillede, nummer/tal

Automatisk genereret beskrivelse---------------------------------------------- Calculating values -----------------------------------------------

Just overshooting 0.5V of range a tiny bit.

Can it ever be negative? In that case , for a being the square root.   
It will never be true, as Vthn is positive.   
   
Now what’s the maximum value of Vo? It’s when M6 is just satisfies overdrive.  
So when the gate source voltage is just about the threshold voltage:   
   
   
   
Therefore  
   
Saying that   
And for m4min to be in saturation = 0.1   
   
   
   
   
And that’s equal to.   
   
Which gives me a relationship between the input transistor and the tail transistor.   
Suggesting that

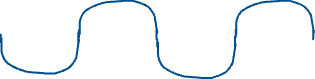
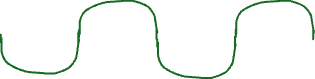
*Ligningen løses for WL\_4 vha. WordMat.*

I prefer the range being larger.   
So I actually want to round down.

Common mode range and source network and input network sized √  
=======================================================  
   
   
=======================================================

*What’s the pmos sizes?*   
It’s a current mirror configuration, set such that Im1 = IO   
   
   
   
   
The maximum current is set to VG6 being just above the threshold voltage.

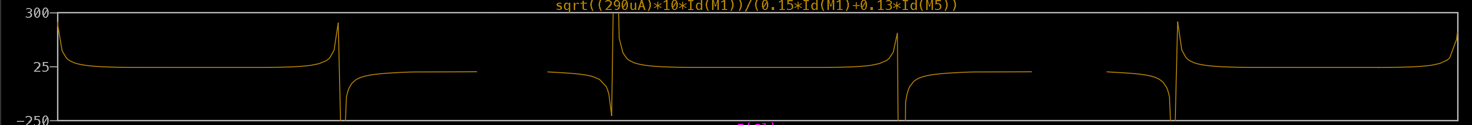
Wow.   
  
  
*What about the tail current?*  
Due to the capacitance at the load, , but as I noticed, the transistor current is much larger than so  
   
Their large signal values are added to  
The itail, but the small signal values are out of 180° out of phase,   
so the subtract each other.   
Then



*What’s my bias resistor then?*Is it ever gonna be negative? Then VGS < VTHn and that means the transistor is off, so no.   
  
And as I’ve wanted my current mirror current source to be made of equal size transistors:

*Ligningen løses for R\_bias vha. WordMat.*

VDS1 could be as low as 0,1. Now seeing that VGS was demanded to be about 1, this prediction is a little off. My testing can then differ a bit.

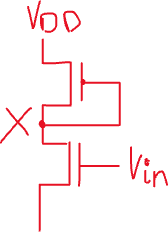
*Et billede, der indeholder skærmbillede

Automatisk genereret beskrivelse* ----------------------------------------------- Testing values ---------------------------------------------------   
   
    
   
 Something is clearly wrong with this setup. The currents aren’t as I predicted and the gain at the output is much smaller.   
Let me try to simulate the gain.

For my setup, it’s suppposed to be 25.

I think I made and error while calculating the pmos sizes. I will revisit all sizes once again:

Step 1, the upper bound for Vin:   
   
   
   
If I were to maximize the upper bound:   
   
   
   
   
  
   
, <- for headroom   
   
   
Thinking 200 is a good biasing current:



Then ensuring that from VDD.

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Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, nummer/tal, linje/række

Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, hvid, linje/række

Automatisk genereret beskrivelseEt billede, der indeholder tekst, Font/skrifttype, skærmbillede, kvittering

Automatisk genereret beskrivelseStarting with some of the criterias:   
   
I can regulate this with the current and with the size of the transistor.



This sets up some criterias, that I can place on the parts of the circuits, coming up.

So let me go through what I currently know.

### Input circuit

#### Requirements

,

#### Equations

#### Tests

### Output circuit

#### Requirements

#### Equations

#### Tests

### Tail current circuit

#### Requirements

#### Equations

#### Tests

Et billede, der indeholder diagram, linje/række, Teknisk tegning, Plan

Automatisk genereret beskrivelseTo start it off, let me look at some common mode voltage ranges:   
For m5 it’s a diode, and for that follows:   
   
And as   
   
Then  
   
   
Giving headroom:   
   
Using that for the upper bound of the input transistor:   
   
   
   
   
   
   
  
Then the upper bound of has been found.

Now for the lower bound.   
   
   
   
Giving headroom:

So my common mode input range:

### Input circuit

#### Requirements

,

#### Et billede, der indeholder tekst, diagram, Font/skrifttype, skærmbillede Automatisk genereret beskrivelseEquations

#### Tests

Et billede, der indeholder tekst, skærmbillede, Kurve, linje/række

Automatisk genereret beskrivelse

And then

So for this dummy circuit I managed to preserve a current of about 50uA, while keeping high voltage at the drain of M1 ensuring that M1 can be in saturation.

### Output circuit

#### Requirements

#### Equations

#### Tests

### Tail current circuit

#### Requirements

#### Equations

#### Tests

Still assuming that , then assuming that the load capacitance is about negligible compared to the transistor current of M2   
   
Just solving for one of the input transistors. The other I say is approximately the same as the other. But creating a relationship to the tail transistor.

But VD4 also sets the lower bound for the common mode voltage range…  
   
Ensuring that:   
   
   
  
Then the maximum value VD4 is

Ensuring the input transistor:   
   
   
   
   
Then the tail transistor:

Solving for the pmos transistors aswell.

The maximum value of makes for .

Setting the transistor dimension equal for the input layer, output layer, and current source layer.  
And then I have:

Et billede, der indeholder tekst, diagram, Plan, skematisk

Automatisk genereret beskrivelseTesting it I only manage 2.4uA through M4.   
Et billede, der indeholder tekst, skærmbillede, Kurve

Automatisk genereret beskrivelse

So I’ll be going back to testing some of the paths.

So far:

### Input circuit

#### Requirements

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#### Equations

#### Tests

### Output circuit

#### Requirements

#### Equations

#### Tests

### Tail current circuit

#### Requirements

#### Equations

#### Tests

Is the tail current capable of running 100uA?

Et billede, der indeholder diagram, tekst, linje/række, Plan

Automatisk genereret beskrivelsePlotting with the current size configuration, I get that about is able to flow through.

Maybe I derived the formula the wrong way?

I derived it from   
   
Let me retry:

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Automatisk genereret beskrivelse   
   
   
That’s a completely different value. Maybe that will work.

That helped, but not quite there.   
Fiddling with the values I get that   
, gets 98.7uA ≈ 100uA.

Implementing it into the Output / input directly makes itail go from 98 -> 82. Just implementing it onto the input layer with VDD directly gets itail go form 98 -> 93.   
This is due to not being met. The voltage is seen to be 0,084V.  
Adjusting the ratio of the input transistor from 0,563 -> 0,7 made all the current run through and satisfy the saturation criteria.

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Automatisk genereret beskrivelseNow adding the pmos network onto it:

The saturation criteria isn’t meet, and its due to the pmos network. Let me tweak their value a little.

I actually realized, that even though I found to be 450, 100 worked almost just as great. Changing the ratio of the pmos didn’t do much else. Adjusting V1 a little more, gives this little more headroom. The saturation criteria for the tail transistor is met for

### Input circuit

#### Requirements

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#### Equations

#### Tests

### Output circuit

#### Requirements

#### Equations

#### Tests

### Tail current circuit

#### Requirements

#### Equations

#### Tests

Now cobbling this to my current mirror source.   
I’ve set , VG4 = 0,66.   
   
   
   
 by a little bit, and that forces changes in the circuit.

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Automatisk genereret beskrivelse



Lifting input transistor size ratio , and increasing the bias transistor to 9000Ω fixes this.

*Now I’ve solved all this for the upper bound, but how does this hold when put at the lower bound?*Recalling boundary equation 5.

1. Figure 1. j\*2f = 1M rad/s [↑](#footnote-ref-1)
2. Figure 2. Analysis after finding error in the way pmoses are setup by default [↑](#footnote-ref-2)
3. Figure 3. (Vin- & Vout, t) at the top, (Vin+ & Vin-, t) at the bottom [↑](#footnote-ref-3)